Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.041”**

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**.041”**

**Top Material: Al**

 **Backside Material: Au**

**Bond Pad Size: B = .0065” X .007” E = .006” X .007”**

**Backside Potential: Collector**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .041” X .041” DATE: 10/4/21**

**MFG: PPC THICKNESS .006” - .012” P/N: 2N3501**

**DG 10.1.2**

#### Rev B, 7/1